

**IN THE CLAIMS**

Claim 1 (currently amended): A low-noise buffer for a digital logic signal, comprising:

an analog amplifier ~~having a unity gain bandwidth substantially greater than a maximum switching rate of the digital logic signal;~~

a converter circuit operative to convert the digital logic signal to a ramp signal provided as an input to the analog amplifier, the ramp signal having a slope determined by a bias current and an input capacitance of the analog amplifier; and

a bias circuit operative to generate the bias current in a manner ensuring that the bias current varies as the input capacitance of the analog amplifier varies ~~due to variations in the manufacturing process of the buffer~~, such that the slope of the ramp signal remains substantially constant ~~despite the variations in the manufacturing process of the buffer~~.

Claim 2 (original): A low-noise buffer according to claim 1, wherein the analog amplifier comprises:

an input stage including a differential pair of PMOS transistors in cascode configuration; and

a differential-to-single-ended, push-pull output stage.

Claim 3 (currently amended): A low-noise buffer according to claim 1, wherein the ramp circuit comprises a switched current source, the magnitude of the current supplied by the switched current source ~~being established by~~ corresponding to the bias current.

Claim 4 (currently amended): A low-noise buffer for a digital logic signal, comprising:

an analog amplifier;

a converter circuit operative to convert the digital logic signal to a ramp signal provided as an input to the analog amplifier, the ramp signal having a slope determined by a bias current and an input capacitance of the analog amplifier; and

a bias circuit operative to generate the bias current in a manner ensuring that the bias current varies as the input capacitance of the analog amplifier varies, such that the slope of the ramp signal remains substantially constant.

~~A low noise buffer according to claim 3,~~ wherein the ramp circuit comprises:

a first switched current mirror operative to generate current of one polarity when the digital logic signal has a first logic value; and

a second switched current mirror operative to generate current of the opposite polarity when the digital logic signal has a second logic value.

Claim 5 (currently amended): A low-noise buffer for a digital logic signal, comprising:

an analog amplifier;

a converter circuit operative to convert the digital logic signal to a ramp signal provided as an input to the analog amplifier, the ramp signal having a slope determined by a bias current and an input capacitance of the analog amplifier; and

a bias circuit operative to generate the bias current in a manner ensuring that the bias current varies as the input capacitance of the analog amplifier varies, such that the slope of the ramp signal remains substantially constant.

~~A low noise buffer according to claim 1,~~ wherein the bias circuit comprises a switched-capacitor resistor across which a predetermined reference voltage is placed to generate the bias current, the switched-capacitor and resistor including a capacitor having capacitance that varies as the input capacitance of the analog amplifier varies due to variations in the manufacturing process of the buffer.